REMARKS

The Office Action mailed May 22, 2002, has been received and reviewed. Claims 1-37 and 52-56 are currently pending in the application. Claims 1-37 and 52-56 stand rejected. Applicants respectfully request reconsideration of the above-referenced application in light of the following remarks.

35 U.S.C. § 103(a) Obviousness Rejections

(A) **Applicable Authority**

The basic requirements of a *prima facie* case of obviousness are summarized in MPEP § 2143 through § 2143.03, *i.e.*, in order "to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success in combining the references. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Further, in establishing a *prima facie* case of obviousness, the initial burden is placed on the examiner. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." *Ex parte Clapp*, 22y USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). See also MPEP § 706.02(j) and § 2142.

The Supreme Court has established the standard of patentability to be applied in obviousness rejections in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966). This standard has been summarized in MPEP § 2141 into four factual inquiries including "(A) determining of the scope and contents of the prior art; (B) ascertaining the differences between the prior art and the claims in

issue; (C) resolving the level of ordinary skill in the pertinent art; and (D) evaluating evidence of secondary considerations." It should be noted that, when applying the required patentability standards of Graham, the basic considerations which apply to obviousness rejections based on 35 U.S.C. § 103 should include the following principles of patent law: "(A) the claimed invention must be considered as a whole; (B) the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; (C) the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and (D) reasonable expectation of success is the standard with which obviousness is determined." *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

(B) **Obviousness rejections in view of U.S. Patent No. 6,337,122 to Grigg et al.**

As set forth in the outstanding Office Action and further discussed herein below, each of the obviousness rejections have been based primarily on U.S. Patent No. 6,337,122 to Grigg et al. (hereinafter the "Grigg reference"). Applicants respectfully submit that, under 35 U.S.C. § 103(c), the obviousness rejections based on the Grigg reference are improper. 35 U.S.C. § 103(c) provides:

> Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

The above-referenced application, which is owned by Micron Technology, Inc., as indicated by the Assignment recorded by the Patent Office on June 8, 2000, at reel/frame: 010870/0153, has an effective filing date of June 8, 2000. The Grigg reference, which was filed on January 11, 2000, but did not issue until January 8, 2002, only qualifies as prior art under 35 U.S.C. § 102(e) and indicates Micron Technology, Inc. to be the assignee thereof. Thus, under the provisions of 35 U.S.C. § 103(c), the Grigg reference cannot be used in a § 103(a) rejection of any of the claims of the above-referenced application.

It is stated in the outstanding Office Action that Applicants have previously provided evidence showing that the invention of the above-referenced application was owned by, or subject to an obligation of assignment to, the same entity as the Grigg reference at the time the invention was made. *See*, Office Action, page 2, paragraph 4 – page 3, paragraph 1. Accordingly, it is recognized by the Examiner that the Grigg reference is disqualified as prior art under 35 U.S.C. § 103(c) as being prior art under 35 U.S.C. § 102(e), (f), or (g) which is used in a rejection of he claims of the above-referenced application under 35 U.S.C. § 103(a). *See id.* However, it is further stated in the outstanding Office Action that the "applied art additionally qualifies as prior art under another subsection of 35 U.S.C. 102 and accordingly is not disqualified as prior art under 35 U.S.C. 103(a)." Office Action, page 2, paragraph 1. There is, however, no indication of which subsection of 35 U.S.C. § 102 is thought to be applicable to the above-referenced application. As the Grigg reference only qualifies as prior art under 35 U.S.C. § 102(e), Applicants respectfully traverse the rejection as hereinafter set forth.

As the Grigg reference is disqualified as being prior art under 35 U.S.C. § 102 (e), (f) and (g), as admitted by the Examiner, a proper rejection may be made under 35 U.S.C. § 103(a) only if the Grigg reference qualifies as prior art under 35 U.S.C. § 102(a), (b), (c), or (d). 35 U.S.C. § 102(a) states that a person shall be entitled to a patent unless:

> the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent . . .

This section sets up two different criteria, at least one of which must have taken place prior to invention by the applicant for patent in order for a reference or activity to qualify as prior art under § 102(a). The first criterion regards knowledge or use by others in this country. As stated in § 2132(I) of the MPEP, "[t]he statutory language 'known or used by others in this country' (35 U.S.C. § 102(a)), means knowledge or use which is accessible to the public." *Carella v. Starlight Archery*, 804 F.2d 135, 231 USPQ 644 (Fed. Cir. 1986). The Examiner has failed to allege or establish any public knowledge or use by others in this country of the invention prior to invention by the applicant. Accordingly, the first criterion of 35 U.S.C. § 102(a) has not been fulfilled.

The second criterion is "patented or described in a printed publication in this or a foreign country". As stated in § 706.02(a)(III) of the MPEP:

> For U.S.C. 102(a) to apply, the reference must have a publication date earlier in time than the effective filing date of the application, and must not be applicant's own work.

Again, the Grigg reference was issued, and published, as a patent in this country on January 8, 2002, well after invention by the applicant, whose effective filing date is June 8, 2000. No prior publication of the Grigg reference in this or a foreign country has been alleged or shown. Nor has any foreign patent has been shown or alleged. Therefore, the second criterion of 35 U.S.C. § 102(a) also has not been satisfied. Accordingly, the Grigg reference does not qualify as prior art under 35 U.S.C. § 102(a).

35 U.S.C. § 102(b) states that a person shall be entitled to a patent unless:

> the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States . . .

Further, as stated in § 706.02(a)(I) of the MPEP, only "[i]f the publication or issue date of the reference is more than one year prior to the effective filing date of the application (MPEP § 706.02), [does] the reference qualif[y] as prior art under § 102(b)."

The date of application for patent in the United States, and the effective filing date, of the above-referenced application is June 8, 2000. The Grigg reference was issued as a patent in this country on January 8, 2002. As stated above, no prior publication of the Grigg reference in this or a foreign country has been alleged or shown, nor has any foreign patent. As such, the Grigg reference does not qualify as prior art under 35 U.S.C. § 102(b).

35 U.S.C. § 102(c) states that a person shall be entitled to a patent unless "he has abandoned the invention . . ." No evidence of abandonment has been shown or alleged. Further, the Grigg reference cannot qualify as prior art under § 102(c) as this section is wholly independent of the actions of persons or entities other than the applicant for patent.

35 U.S.C. § 102(d) states that a person shall be entitled to a patent unless:

> the invention was first patented or caused to be patented, or was the subject of an inventor's certificate, by the applicant or his legal representatives or assigns in a foreign country prior to the date of the application for patent in this country on an application for patent or inventor's certificate filed more than twelve months before the filing of the application in the United States . . .

This section sets forth four conditions which, if all are present, establish a bar against the granting of a United States Patent. First, the foreign application must be filed more than 12 months before the effective U.S. filing date. Second, the foreign application must have been filed by the same applicant as in the United States or by his or her legal representatives or assigns. Third, the foreign patent or inventor's certificate must be actually granted before the U.S. filing date (although it need not be published). And fourth, the same invention must be involved. *See*, MPEP § 2135.

Clearly the Grigg reference does not qualify as prior art under 35 U.S.C. § 102(d) because, among other reasons, it is not a foreign application, was not filed more than 12 months before the U.S. filing date of the above-referenced application and it was not filed by the same applicant.

Accordingly, the 35 U.S.C. § 103(a) obviousness rejections of claims 1-37 and 52-56 are improper because the only subsection of § 103 under which the Grigg reference qualifies as prior art is § 102(e). Based upon § 103(c), § 102(e) prior art shall not preclude patentability under 35 U.S.C. § 103 in this circumstance. As such, withdrawal of the 35 U.S.C. § 103(a) rejections that are at least partially based on the Grigg reference is respectfully requested.

(C) **Obviousness Rejection Based on U.S. Patent No. 6,337,122 to Grigg et al. in View of U.S. Patent No. 6,284,563 to Fjelstad**

Claims 1 through 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Grigg reference in view of U.S. Patent No. 6,284,563 to Fjelstad (hereinafter the "Fjelstad reference"). Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicants respectfully submit that, besides the inappropriateness of using the Grigg reference to find obviousness in the instant invention under 35 U.S.C. § 103(a) as explained

hereinabove in Subsection (B), as it will be further substantiated below, the Fjelstad reference does not support a *prima facie* case of obviousness of the present invention.

The Fjelstad reference relates to a process of creating a compliant chip package on the face surface of a single die, multiple die, or undiced silicon wafer which may be subsequently diced into individual packaged chips. (Col. 8, lines 13-19). A dielectric passivation layer 130 is deposited onto or adhered to the face surface 120 of a single semiconductor chip 100, covering the face surface 120 while leaving the chip contacts 110 exposed so that a bond ribbon may be plated thereon. Several preferred methods to form the passivation layer 130 are disclosed, including: *(i)* spinning onto and building up passivation material to a planar sheet-like form to be laminated to the face surface 120 using adhesives; *(ii)* exposing and developing photo-imagable material deposited on the face surface 120 and later removing the leftover material from the unexposed areas by use of a pulse of directed energy; and *(iii)* laminating the chip 100 with a continuous dielectric sheet already having set contact holes. Next, a compliant layer 140, which is stenciled, screened or transfer molded using a curable liquid, is deposited or laminated onto the exposed surface of the passivation layer 130. A plating seed layer 150 is next deposited atop the aforementioned assembly, typically using a sputtering operation, and a photoresist 160 is then applied to the exposed top surfaces of the assembly and exposed and developed such that bond ribbons 170 may be plated within defined areas to form conductive paths electrically connecting the chip contacts 110 near a first end region of the ribbons 170 to terminals 175 comprising the second end region of the ribbons 170. A dielectric layer 180 is then deposited or laminated over the top of the assembly so that only the terminals 175 are exposed. The dielectric layer may be comprised of a screened, exposed and developed, or laminated sheet of photoresist material, or may be comprised of paralene, epoxy resin, polyimide resin, or fluoropolymer which is deposited or laminated on to the assembly. The terminals 175 may then be electrically connected to a circuitized substrate, such as a printed wiring board. (Col. 8, line 20 – col. 10, line 44).

Alternate embodiments are disclosed with teach *(i)* different methods to deposit encapsulant materials to the face of the substrate, including the use of a fixture (col. 11, lines 23-27) or a machine

(col. 11, lines 30-35) to flow a liquid material; *(ii)* the use of a conductive material to form ribbons 170 by sputtering or depositing it across the exposed surface of the assembly and then etching the deposited material using industry standard photolithographic techniques (col. 11, lines 42-60); *(iii)* the use of molds and curable liquids for depositing the different layers in the assembly (col. 12, lines 24-60); and *(iv)* the use of one or more non-selective deposition techniques, such as electroless plating or sputtering of a conductive layer over the assembly, to make bond ribbons 170 with or without an additional non-selective electroplating step, followed by selective etching of the conductive layer to provide electrically isolated bond ribbons (col. 12, line 37 – col. 13, line 27).

As to the obviousness rejections of independent claims 1 and 12 based upon the Fjelstad reference, Applicants respectfully submit that a *prima facie* case of obviousness cannot be supported by this prior art reference. First, it is respectfully submitted that one of ordinary skill in the art would not have been motivated by the teachings of the Fjelstad reference, or the knowledge that was generally available in the art before the filing date of the above-referenced application, to modify the teachings of the Fjelstad reference in the manner necessary to achieve the method of fabricating a protective layer on a semiconductor device as recited in independent claim 1, nor the method of forming a layer of protective material on a specified area on an active surface of one or more selected dice of a plurality of semiconductor dice of a wafer as recited in independent claim 12. The Fjelstad reference is relied upon merely for its description of "a process where a dielectric protective compliant layer is placed over a semiconductor chip" having at least one bond pad. Office Action, page 3, paragraph 4-page 4, paragraph 1. It is respectfully submitted that modifying such process to achieve the methods of independent claims 1 and 12, particularly "selectively altering the state of . . . protective material . . . to at least a semisolid state . . .", is not within the purview of one of ordinary skill in the art.

Second, it is respectfully submitted that the Fjelstad reference does not teach or suggest each and every element of the rejected claims. In particular, Fjeslstad neither teaches nor suggests "selectively altering the state of . . . protective material . . . to at least a semisolid state . . ." Nor is it

alleged that the reference does so in the absence of the Grigg reference which, as stated previously, is inappropriate prior art.

As such, independent claims 1 and 12 are believed to be in condition for allowance. Claims 2 through 11 and 13 through 23 each depend, either directly or indirectly, from one of claims 1 and 12 and, thus, are believed to be in condition for allowance for at least the above-stated reasons. Accordingly, withdrawal of the § 103(a) rejection of claim 1 through 23 is respectfully requested.

(D) **Obviousness Rejection Based on U.S. Patent No. 6,337,122 to Grigg et al. in View of U.S. Patent No. 6,284,563 to Fjelstad and in Further View of U.S. Patent No. 5,897,338 to Kaldenberg**

Claims 24 through 37 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Grigg reference in view of the Fjelstad reference, and in further view of U.S. Patent No. 5,897,338 to Kaldenberg (hereinafter the "Kaldenberg reference"). Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicants respectfully submit that, besides the inappropriateness of using the Grigg reference to find obviousness in the instant invention under 35 U.S.C. § 103(a), as explained hereinabove in Subsection (B), as it will be further substantiated below, the Fjelstad reference and the Kaldenberg reference, individually or in any combination thereof, do not support a *prima facie* case of obviousness of the present invention.

The Fjelstad reference has been discussed hereinabove in Subsection (C). The Kaldenberg reference relates to a method for encapsulating an integrated semi-conductor circuit (die) comprising the steps of *(i)* mounting the semi-conductor circuit onto the surface of a lead frame; *(ii)* attaching connecting wires between the contact surfaces of the semiconductor circuit and selected parts of the lead frame; and *(iii)* producing a plastic housing by means of a mold that at least encapsulates the semiconductor circuit, the support surface, the bonding wires, and part of the lead frame. (Col. 1, lines 6-16). This encapsulation around the integrated semi-conductor circuit, which comprises optical-electronic components, is such that the resulting housing should have a cavity that gives an open connection between the outside world and the active area of the die. If this cavity should be

closed, it should be closed with a window that is opaque for radiation (both in the visible part of the spectrum as well as in the infrared or ultraviolet parts of the spectrum). (Col. 1, lines 26-34). A chip 12 is attached to the central section of a lead frame 10b by the bonding wires 14a and 14b between the various contact pins and the connecting surfaces on the chip. In the disclosed embodiment, the mold comprises a bottom part 16 and a cover part 18. An opening 20 is made in the cover part 18 above the semiconductor circuit 12. The opening 20 is closed by means of an extending part 22 with a cross-sectional shape corresponding to the shape of the opening 20. Preceding the insertion of the part 22, a certain amount of heat resistant deformable material 23, in the form of a ring or a continuous layer, is applied to the underside of part 22. Preferably, the deformable material consists of a gel, especially a silicon gel. Thereafter, an epoxy or resin 24 is injected in the free space in the mold to create the encapsulation. After at least partly hardening of the now encapsulated semiconductor circuit, part 22 and the deformable material 23 are removed from the mold, resulting in a semiconductor circuit that is partly encapsulated with a part of its upper surface still left free. Due to the shape of part 22, the resulting opening above chip 12 has a stepwise shape suitable for mounting a window 26 by using a suitable adhesive 28. (Col. 3, lines 9-61).

As to the obviousness rejections of independent claims 24 and 33 based upon the Fjelstad reference in further view of the Kaldenberg reference, Applicants respectfully submit that a *prima facie* case of obviousness cannot be supported by these prior art references. First, it is respectfully submitted that one of ordinary skill in the art would not have been motivated by the teachings of the Fjelstad reference and the Kaldenberg reference, or the knowledge that was generally available in the art before the filing date of the above-referenced application, to modify the teachings of the Fjelstad reference and the Kaldenberg reference in the manner necessary to achieve the method for forming a protective layer on a selected portion of a surface of a semiconductor die, as recited in independent claim 24, or the method for forming a protective layer on a selected portion of an active surface of a semiconductor dice of a wafer, as recited in independent claim 33. The Fjelstad reference is relied upon merely for its description of "a process where a dielectric protective compliant layer is placed over a semiconductor chip, having at least one bond pad and other active areas for device

development." Office Action, page 5, paragraph 5. The Kaldenberg reference is relied upon for its description of a "process that encapsulates a semiconductor chip with a lead frame." Office Action, page 6, lines 1-2. It is respectfully submitted that modifying such processes to achieve the methods of independent claims 24 and 33, particularly the "subjecting selected portions of [a] layer to a controllable beam of radiation to change [a] liquid resin . . . to an at least semisolid state" of claim 24 and the "subjecting at least one selected portion of [a] liquid resin . . . to a discrete beam of focused radiation to alter said liquid resin . . . to at least a semisolid state . . ." of claim 33, is not within the purview of one of ordinary skill in the art.

Second, it is respectfully submitted that the Fjelstad reference and the Kaldenberg reference, whether taken individually or alone, do not teach or suggest each and every element of the rejected claims. With respect to claim 24, Fjelstad and Kaldenberg both lack any teaching or suggestion of "subjecting selected portions of [a] layer to a controllable beam of radiation to change [a] liquid resin . . . to an at least semisolid state." As for claim 33, neither Fjelstad nor Kaldenberg teaches or suggests "subjecting at least one selected portion of [a] liquid resin . . . to a discrete beam of focused radiation to alter said liquid resin . . . to at least a semisolid state . . ." Nor is it alleged that they do so in the absence of the Grigg reference which, as stated previously, is inappropriate prior art.

As such, independent claims 24 and 33 are believed to be in condition for allowance. Claims 25 through 32 and 34 through 37 each depend, either directly or indirectly, from one of claims 24 and 33 and, thus, are believed to be in condition for allowance for at least the above-stated reasons. Accordingly, withdrawal of the § 103(a) rejection of claim 24 through 37 is respectfully requested.

(E) **Obviousness Rejection Based on U.S. Patent No. 6,337,122 to Grigg et al. in View of U.S. Patent No. 6,284,563 to Fjelstad and in Further View of U.S. Patent No. 6,045,655 to DiStefano et al.**

Claims 52 through 56 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Grigg reference in view of the Fjelstad reference, and in further view of U.S. Patent No. 6,045,655 to DiStefano et al. (hereinafter the "DiStefano reference"). Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicants respectfully submit that, besides the inappropriateness of using the Grigg reference to find obviousness in the instant invention under 35 U.S.C. § 103(a) as explained hereinabove in Subsection (B), as it will be further substantiated below, the Fjelstad reference and the DiStefano reference, individually or in any combination thereof, do not support a *prima facie* case of obviousness of the present invention.

The Fjelstad reference has been discussed hereinabove in Subsections (C). The DiStefano reference relates to prefabricated connection components and a method of bonding such connection components to chips to form subassemblies. The connection components of the DiStefano reference incorporate a support structure 20 which includes a thin, flexible top layer 22 and a compliant bottom layer 24. (Col. 6, lines 30-34). The bottom layer 24 defines the bottom surface of the support structure 20 and the bottom layer 24 of each support structure 20 is bonded to the top, flexible layer 22 of such support structure 20 by a substantially non-releasable bond 23, *e.g.*, an adhesive. (Col. 6, lines 36-40). The top layer 22 and the bottom layer 24 are generally rectangular and substantially coextensive with one another. The top layer 22 is formed integrally with a support or carrier tape 28. The carrier tape 28, in turn, is formed integrally with additional top layers 22 of other support structures 20 of additional connection components. Each top layer 22 is separated from the surrounding portions of the tape 28 by a series of continuous gaps extending around the top layer 22. (Col. 6, line 66-col. 7, line 11).

Each connection component is provided with a set of electrical terminals 34 mounted on the top surface of the support structure top layer 22. The terminals 24 are arranged in a pattern suitable for bonding to a substrate. (Col. 7, lines 12-15). Each terminal 24 is connected to an elongated metallic electrical lead 36 extending from the terminal on the top layer 22. Each lead 36 has a connection section 38 extending across one of the gaps 32. A distal end of each connection section 38, remote from the support section 20 and the top layer 22, is connected via a frangible section 40 to a bus structure 42 anchored on tape 28 and surrounding the gaps 32. (Col 7, lines 20-27). Each connection component further includes an adhesive 44 disposed on the bottom surface of the bottom layer 24 in a pattern incorporating a plurality of adhesive masses. The adhesive masses include a

central mass 46 disposed adjacent the center of the bottom surface and a plurality of elongated masses 48 extending radially outwardly from the central mass 46 in a generally star-like pattern. The regions of the bottom surface 25 between the adhesive masses are substantially devoid of the adhesive. These regions thus constitute depressions or grooves 47 between the elongated adhesive masses 48. (Col. 7, lines 34-47).

In a method of the DiStefano reference, the prefabricated connection components discussed above are bonded to chips 50 to form subassemblies. (Col. 8, lines 27-30). The chip 50 is heated to a temperature above the activation temperature of the adhesive 44 while the chip is out of contact with the support structure and the adhesive. (Col. 8, lines 42-46). While the chip is at its elevated temperature, the connection component is aligned with the chip so that the support structure 20 overlies the chip, with the bottom surface of the support structure bottom layer facing downwardly towards the chip top surface. During this process, the connection component may be handled and supported through the tape 28, such as with a support 62. (Col. 8, lines 52-58). A conventional, automated pattern recognition system 64 and associated conventional movement and positioning devices are used to register support 62, tape 28 and, hence, the connection component with the chip. Thus the connection component is shifted in horizontal directions, parallel to the top surface of the chip, until the connection sections 38 of the connection component leads are disposed vertically above the contacts 54 of the chip, in alignment therewith. This may be accomplished by moving the support 62, the tape 28 and the connection component support structure 20, or by moving the hot plate on which the chip may be placed, or both under the control of a pattern recognition device. (Col. 8, line 61 — col. 9, line 5). After the connection component and the chip have been aligned in this manner, the connection component and the chip are advanced vertically toward one another and bonded. (Col. 9, lines 10-13). After the bonding process, the tape 28 is removed and the assembly including the connection component and the chip is cooled, typically to room temperature. In this condition, the adhesive 44 retains the connection component support structure 20 on the top surface of the chip and provides a substantially void-free interface between the two components. (Col. 10, lines 21-27).

As to the obviousness rejection of independent claim 52 based upon the Fjelstad reference further in view of the DiStefano reference, Applicants respectfully submit that a *prima facie* case of obviousness cannot be supported by these prior art references. First, it is respectfully submitted that one of ordinary skill in the art would not have been motivated by the teachings of the Fjelstad reference and the DiStefano reference, or the knowledge that was generally available in the art before the filing date of the above-referenced application, to modify the teachings of the Fjelstad reference and the DiStefano reference in the manner necessary to achieve the method for securing a component of a semiconductor device assembly to another component of the semiconductor device assembly, as recited in independent claim 52. The Fjelstad reference is relied upon merely for its description of "a process where a dielectric protective compliant layer is placed over a semiconductor chip, having at least one bond pad and other active areas for device development." Office Action, page 7, paragraph 3. The DiStefano reference is relied upon for its description of a process of providing an adhesive or compliant layer to semiconductor chips mounted on a package and the alignment of components thereof. Office Action, page 7, paragraph 3. It is respectfully submitted that modifying such processes to achieve the method of independent claim 52, particularly providing a component including at least one support structure "comprising a plurality of superimposed, contiguous, mutually adhered layers of material . . .", is not within the purview of one of ordinary skill in the art.

Second, it is respectfully submitted that the Fjelstad reference and the DiStefano reference do not teach or suggest each and every element of the rejected claims. For example, both Fjelstad and DiStefano lack any teaching or suggestion of providing a component that includes at least one support structure "comprising a plurality of superimposed, contiguous, mutually adhered layers of material . . ." Nor is it alleged that the references do so in the absence of the Grigg reference which, as stated previously, is inappropriate prior art.

As such, independent claim 52 is believed to be in condition for allowance. Claims 53 through 56 each depend, either directly or indirectly, from claim 52 and, thus, are believed to be in condition for allowance for at least the above-stated regions. Accordingly, withdrawal of the § 103(a) rejection of claim 52 through 56 is respectfully requested.

CONCLUSION

Claims 1 through 37 and 52 through 56 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,

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